Listing to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously presented) A method for use in a decoder, the method comprising the steps of:

delaying received encoded symbol data to produce delayed data;

re-encoding decoded symbol representative data to produce re-encoded symbol data;

feed-forward processing said re-encoded symbol data to produce difference data representative of a difference between successive symbols of said re-encoded symbol data; and

deriving decoded symbol data using said delayed data and said difference data.

2. (Original) A method according to claim 1, wherein

said feed-forward processing is exclusive of feed-back processing.

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3. (Original) A method according to claim 1, wherein

said feed-forward processing prevents error accumulation induced by error-propagation resulting from feed-back processing.

4. (Previously presented) A method according to claim 1, including the steps of

comparing candidate values representative of distance between said delayed data and said difference data, to determine minimum distance values, and

resolving equality between determined minimum distance values in response to a prior delayed and fed back comparison representative output.

5. (Previously presented) A decoder comprising:

a delay element for delaying received encoded symbol data to produce delayed data;

a re-encoder for re-encoding decoded symbol representative data to produce re-encoded symbol data; and

a processor for,

feed-forward processing said re-encoded symbol data to produce difference data representative of a difference between successive symbols of said re-encoded symbol data; and

deriving decoded symbol data using said delayed data and said difference data.

6. (Original) A decoder according to claim 5, wherein

said feed-forward processing is exclusive of feed-back processing.

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7. (Original) A decoder according to claim 5, wherein

said feed-forward processing prevents error accumulation induced by error-propagation resulting from feed-back processing.

8. (Previously presented) A decoder according to claim 5, wherein

said processor includes a decision processor for deriving said decoded symbol data by computing an absolute distance between said difference data and a corresponding delayed received encoded symbol of said delayed data.

9. (Original) A decoder according to claim 5, wherein said processor includes,

a decision processor for deriving said decoded symbol data by computing an absolute distance using said difference data and said delayed data, and

a comparator for comparing computed absolute distance values to determine a minimum symbol difference value.

10. (Previously presented) A decoder according to claim 5, wherein said processor includes,

a decision processor for comparing candidate values representative of distance between said delayed data and said difference data, to determine minimum distance values and resolving equality between determined minimum distance values in response to a prior delayed and fed back comparison representative output.

11. (Original) A decoder according to claim 10, wherein

said prior delayed fed back comparison representative output is only used in the case of equality between candidate minimum distance values.

12. (Original) A decoder according to claim 5, wherein

said processor derives decoded symbol data in a partial response system.

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13. (Previously presented) A decoder comprising:

a delay element for delaying received encoded symbol data to produce delayed data;

a re-encoder for re-encoding decoded symbol representative data to produce re-encoded symbol data; and

a processor including,

a feed-forward processor for processing said re-encoded symbol data exclusively of feed-back processing in order to produce difference data representative of a difference between successive symbols of said re-encoded symbol data; and

a decision processor for deriving said decoded symbol data by computing an absolute distance using said difference data and said delayed data.

14. (Original) A decoder according to claim 13, wherein said processor includes,

a comparator for comparing computed absolute distance values to determine a minimum symbol difference value.

15. (Previously presented) A decoder according to claim 13, wherein said processor includes,

a comparator for comparing candidate values representative of distance between, said delayed data and said difference data, to determine minimum distance values and resolving equality between determined minimum distance values in response to a prior delayed and fed back comparison representative output.

16. (Original) A decoder according to claim 15, wherein said processor uses a different configuration in resolving equality between candidate distance values than is used for deriving said difference data.

Claim 17 (Canceled).

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18. (Previously presented) A trellis decoding apparatus comprising:

a delay element for delaying received trellis encoded data to produce delayed data;

a re-encoder for re-encoding decoded trellis encoded data using decision data associated with trellis state transitions in response to said trellis encoded data to produce re-encoded subset data;

a processor for,

feed-forward processing said re-encoded subset data to produce subset difference data representative of a difference between successive symbols using past subset outputs in an error propagation-free, feed-forward configuration; and

deriving decoded symbol data using said delayed data and said difference data.

19. (Original) A decoder according to claim 18, wherein

said error propagation-free feed-forward configuration of said processor derives decoded symbol data using past subset outputs instead of decoded bits themselves.